CHAPTER 3

Discrete Transistor Circuitry

This chapter deals with small-signal design using discrete transistors, specifically BJTs. Many things found in standard textbooks are skated over quickly. It concentrates on audio issues, and gives information that I do not think appears anywhere else, including the distortion behavior of various configurations.

Why Use Discrete Transistor Circuitry?

Circuitry made with discrete transistors is not obsolete. It is appropriate when:

1. a load must be driven to higher voltages than the op-amp can sustain between the supply rails. Op-amps are mostly restricted to supply voltages of ± 18 or ± 20 V. Hybrid-construction amplifiers, typically packaged in TO-3 cans, will operate from rails as high as ± 100 V, but they are very expensive, and not optimized for audio use in parameters like crossover distortion. Discrete op-amps provide a viable alternative;

2. a load requires more drive current, because of its low impedance, than an op-amp can provide without overheating or current limiting, e.g. any audio power amplifier;

3. the best possible noise performance is required. Discrete bipolar transistors can outperform op-amps, particularly with low source resistances, say 500 Ω or less. The commonest examples are moving-coil head amps and microphone preamplifiers. These almost invariably use a discrete input device or devices, with the open-loop gain (for linearity) and load-driving capability provided by an op-amp which may itself have fairly humble noise specs;

4. the best possible distortion performance is demanded. Most op-amps have Class-B or -AB output stages, and many of them (though certainly not all) show clear crossover artefacts on the distortion residual. A discrete op-amp can dissipate more power than an IC, and so can have a Class-A output stage, sidestepping the crossover problem completely;

5. it would be necessary to provide a low-voltage supply to run just one or two op-amps. The cost of extra transformer windings, rectifiers, reservoirs, and regulators will buy a lot of discrete transistors. For example, if you need a buffer stage to drive a power amplifier from a low impedance, it may be more economical, and save space and weight, to use a discrete

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emitter-follower running from the same rails as the power amplifier. In these days of auto-insertion; fitting the extra parts on the PCB will cost very little;

6. purely for marketing purposes, as you think you can mine a vein of customers that don't trust op-amps.

When studying the higher reaches of discrete design, the most fruitful source of information is paradoxically papers on analog IC design. This applies with particular force to design with BJTs. The circuitry used in ICs can rarely be directly adapted for use with discrete semiconductors, because some features such as multiple collector transistors and differing emitter areas simply do not exist in the discrete transistor world; it is the basic principles of circuit operation that can be useful. A good example is a paper by Erdi, dealing with a unity-gain buffer with a slew rate of 300 V/μs [1]. Another highly informative discourse is by Barry Hilton [2], which also deals with a unity-gain buffer.

Bipolars and FETs

This chapter only deals with bipolar transistors. Their high transconductance and predictable operation make them far more versatile than FETs. The highly variable V_g values of an FET can be dealt with by expedients such as current-source biasing, but the low gain, which means low feedback and poor linearity, remains a problem. FETs have their uses when super-high input impedances are required, and an example of a JFET working with an op-amp that provides loop gain can be found in Chapter 13 on microphone amplifiers.

Bipolar Junction Transistors

There is one thing to get straight first: *the bipolar junction transistor is a voltage-operated device*.

What counts is the base-emitter voltage, or V_{be}. Certainly a BJT needs base current to flow for it to operate, but this is really an annoying imperfection rather than the basis of operation. I appreciate this may take some digesting; far too many discussions of transistor action say something like 'a small current flowing into the base controls a much larger current flowing into the collector'. In fact the only truly current-operated amplifying device that comes to mind is the Hall-effect multiplier, and you don't come across those every day. I've certainly never seen one used in audio – could be a market niche there.

Transistor operation is thus: if the base is open-circuit, then no collector current flows, as the collector–base junction is effectively a reverse-biased diode, as seen in Figure 3.1. There is

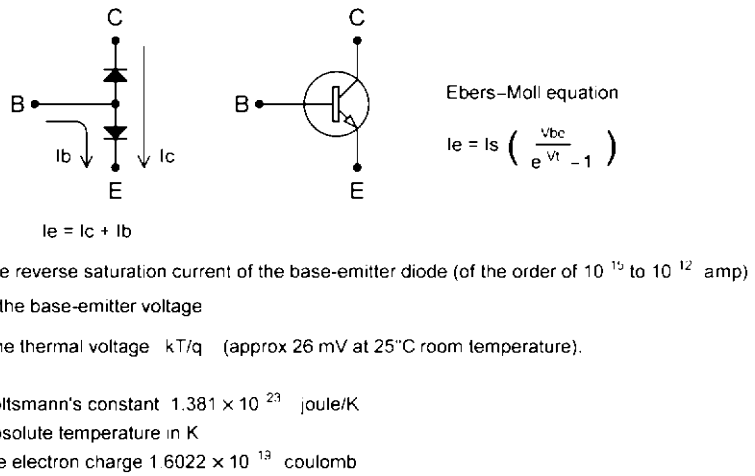

Figure 3.1: Current flow through a bipolar transistor and the fundamental transistor equation

a little leakage through from the collector to the emitter, but with modern silicon BJTs you can usually ignore it.

When the base is forward biased by taking it about 600 mV above the emitter, charge carriers are launched into the base region. Since the base region is narrow, the vast majority shoot through into the collector, to form the collector current I_c. Only a small proportion of these carriers are snared in the base and become the base current I_b, which is clearly a result and not the cause of the base-emitter voltage. I_b is normally just a nuisance.

The Transistor Equation

Every bipolar transistor obeys the Ebers–Moll transistor equation shown in Figure 3.1 with startling accuracy over nine or ten decades of I_c, which is a pretty broad hint that we are looking at the fundamental mechanism. In contrast, beta varies with I_c, temperature, and just about everything else you can think of. The collector current is to a first approximation independent of collector voltage – in other words, it is a current-source output. The qualifications to this are as follows:

1. This only holds for V_{ce} above, say, 2 V.
2. It is not a perfect current source; even with a high V_{ce}, I_c increases slowly with V_{ce}. This is called the Early Effect, after Jim Early [3], and has nothing to do with timing or punctuality. It is a major consideration in the design of stages with high voltage gain. The same effect when the transistor is operated in reverse mode – a perversion that will not concern us here – has sometimes been called the Late Effect. Ho-ho.

Beta

Beta (or h_{fe}) is the ratio of the base current I_b to the collector current I_c. It is not a fundamental property of a BJT. Never design circuits that depend on beta, unless of course you're making a transistor tester.

Here are some of the factors that affect beta. This should convince you that it is a shifty and thoroughly untrustworthy parameter:

- Beta varies with I_c. First it rises as I_c increases, reaching a broad peak, and then it falls off as I_c continues to increase.
- Beta increases with temperature. This seems to be relatively little known. Most things, like leakage currents, get worse as temperature increases, so this makes a nice change.
- Beta is lower for high-current transistor types.
- Beta is lower for high V_{ceo} transistor types. This is a major consideration when you are designing the small-signal stages of power amplifiers with high supply rails.
- Beta varies widely between nominally identical examples of the same transistor type.

A very good refutation of the beta-centric view of BJTs is given by Barrie Gilbert [4].

Unity-Gain Buffer Stages

A buffer stage is used to isolate two portions of circuitry from each other. It has a high input impedance and low output impedance; typically it prevents things downstream from loading things upstream. The use of the word 'buffer' normally implies 'unity-gain buffer' because otherwise we would be talking about an amplifier or gain stage. The gain with the simpler discrete implementations is in fact slightly less than 1. The simplest discrete buffer circuit-block is the one-transistor emitter-follower; it is less than ideal both in its mediocre linearity and its asymmetrical load-driving capabilities. If we permit ourselves another transistor, the complementary feedback pair (CFP) configuration gives better linearity. Both versions can have their load-driving performance much improved by replacing the emitter resistor with a constant-current source or a push–pull Class-A output arrangement.

If the CFP stage is not sufficiently linear, the next stage in sophistication is to combine an input differential pair with an output emitter-follower, using three transistors. This arrangement, often called the Schlotzaur configuration [5], can be elaborated until it gives a truly excellent distortion performance. Its load-driving capability can be enhanced in the same way as in the simpler configurations.

The Simple Emitter-Follower

The simplest discrete circuit-block is the one-transistor emitter-follower. This count of one does not include extra transistors used as current sources, etc., to improve load-driving ability. It does not have a gain of exactly 1, but it is usually pretty close.

Figure 3.2 shows a simple emitter-follower with a 2k7 emitter resistor R2, giving a quiescent current of 8.8 mA with ±24 V supply rails. Biasing is by a high-value resistor R1 connected to 0 V. Note the polarity of the output capacitor; the output will sit at about −0.6 V due to the V_{be} drop, plus a little lower due to the voltage drop caused by the base current I_b flowing through R1.

The input impedance is approximately that of the emitter resistor in parallel with an external loading on the stage multiplied by the transistor beta:

$$R_{in} = \beta(R_e \| R_{load}) \qquad \text{(Equation 3.1)}$$

Don't expect the output impedance to be as low as an op-amp with plenty of negative feedback (NFB). The output impedance is approximately that of the source resistance divided by beta:

$$R_{out} = R_s/\beta \qquad \text{(Equation 3.2)}$$

The gain of an emitter-follower is always slightly less than unity, because of the finite transconductance of the transistor. Essentially the intrinsic emitter resistance r_e (not to be confused with the physical component Re) forms a potential divider with the output load. It is simple to work out the small-signal gain at a given operating point. The value of r_e is given by

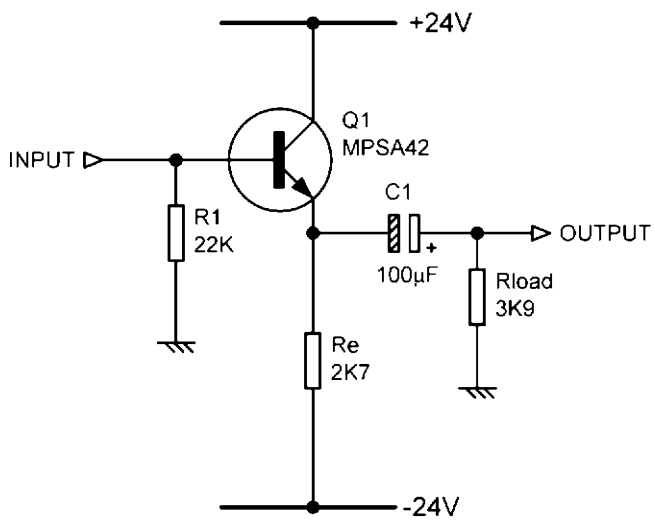

Figure 3.2: The simple emitter-follower circuit running from ±24 V supply rails

$25/I_c$ (for I_c in mA). Since the value of r_e is inversely proportional to I_c, it varies with large signals, and it is one cause of the rather imperfect linearity of the simple emitter-follower. Heavier external loading increases the modulation of I_c, increases the gain variation, and so increases distortion.

Figure 3.2 shows the emitter-follower with an AC-coupled load. Its load-driving capability is not very good. While the transistor can, within limits, source as much current as required into the load, the current-sinking ability is limited by the emitter resistor Re, which forms a potential divider with the load resistance R_{load}. With the values shown here, negative clipping occurs at about −10 V, severely limiting the maximum output amplitude. The circuit shows a high-voltage low-beta transistor type running from ±24 V rails, to give worst-case performance results and to exploit the ability of discrete circuitry to run from high-voltage rails.

The simple emitter-follower has several factors that affect its distortion performance:

- Distortion is reduced as the emitter resistor is reduced, for a given load impedance.
- Distortion is reduced as the DC bias level is raised above the mid-point.
- Distortion increases as the load impedance is reduced.
- Distortion increases monotonically with output level.
- Distortion does *not* vary with the beta of the transistor. This statement assumes low-impedance drive, which may not be the case for an emitter-follower used as a buffer. If the source impedance is significant then beta is likely to have a complicated effect on linearity – and not always for the worse.

Emitter-follower distortion is mainly second harmonic, except when closely approaching clipping. This is entirely predictable, as the circuit is asymmetrical. Only symmetrical configurations, such as the differential pair, restrict themselves to generating odd harmonics only, and then only when they are carefully balanced [6]. Symmetry is often praised as desirable in an audio circuit, but this is subject to Gershwin's Law: 'It ain't necessarily so'. Linearity is what we want in a circuit, and symmetry is not necessarily the best way to get it.

Because the distortion is mostly second harmonic, its level is proportional to amplitude, as seen in Figure 3.3. At 2 Vrms with no load it is about 0.006%, rising to 0.013% at 4 Vrms. External loading always makes the distortion worse, and more rapidly as the amplitude approaches the clipping point; the THD is more than doubled from 0.021% to 0.050% at 6 Vrms, just by adding a light 6k8 load. For these tests Re was 2k7, as in Figure 3.2.

For both the emitter-follower (EF) and CFP circuits, distortion is flat across the audio band so no THD/frequency plots are given.

Insight into what's happening can be gained by using SPICE to plot the incremental gain over the output swing, as in Figure 3.4. As loading increases the curvature of the gain characteristic

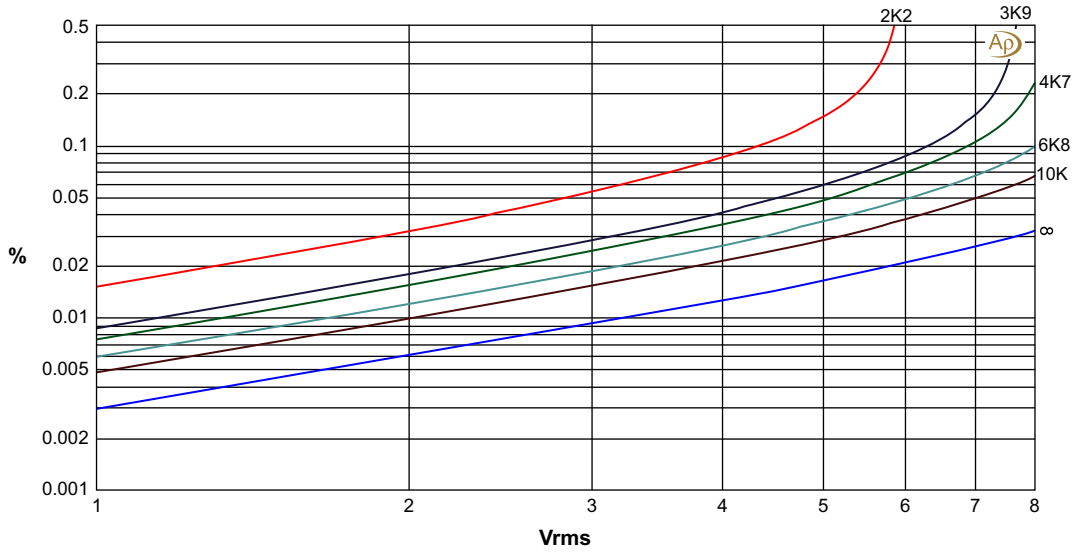

Figure 3.3: How various external loads degrade the linearity of the simple emitter-follower. Re = 2k7

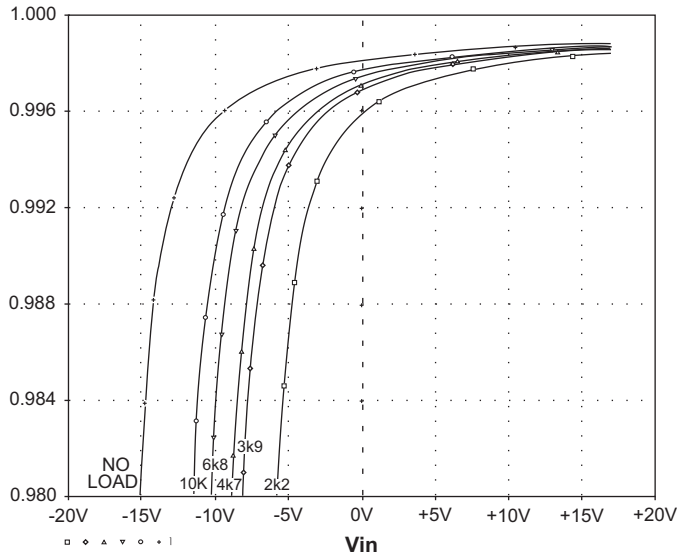

Figure 3.4: Incremental gain of the circuit in Figure 3.2, with a different loads. A distortionless circuit would have constant gain and so give horizontal lines. SPICE simulation

becomes greater for a given voltage swing. It is obvious that the circuit is much more linear on the positive side of 0 V, explaining why emitter-followers give less distortion when biased above the mid-point. This trick can be very useful if the full output swing is not required.

Most amplifier stages are biased so the quiescent output voltage is at the mid-point of the operating region, to allow the maximum symmetrical voltage swing. However, the asymmetry of the simple emitter-follower's output current capability means that if there is significant loading, a greater symmetrical output swing is often possible if the stage is biased positive of 0 V. If the output is loaded with 2k2, negative clipping occurs at −8 V, which allows a maximum output amplitude of only 5.6 Vrms. The unloaded output capability is about 12 Vrms. If the bias point is raised from 0 to +5 V, the output capability becomes roughly symmetrical and the maximum amplitude is increased to 9.2 Vrms. Don't forget to turn the output capacitor around.

The measured noise output of this stage with a 40 Ω source resistance is a commendably low −122.7 dBu (22 Hz to 22 kHz) but with a base-stopper resistor (see below) of 1 kΩ this degrades to −116.9 dBu. A higher stopper of 2k7 gives −110.4 dBu.

The Constant-Current Emitter-Follower

The simple emitter-follower can be greatly improved by replacing the sink resistor Re with a constant-current source, as shown in Figure 3.5. The voltage across a current source does not (to a first approximation) affect the current through it, so if the sink current is large enough a load can be driven to the full voltage swing in both directions.

The current source Q2 is biased by D1, D2. One diode cancels the V_{be} drop of Q2, while the other sets up 0.6 V across the 100 Ω resistor R2, establishing the quiescent current at 6 mA.

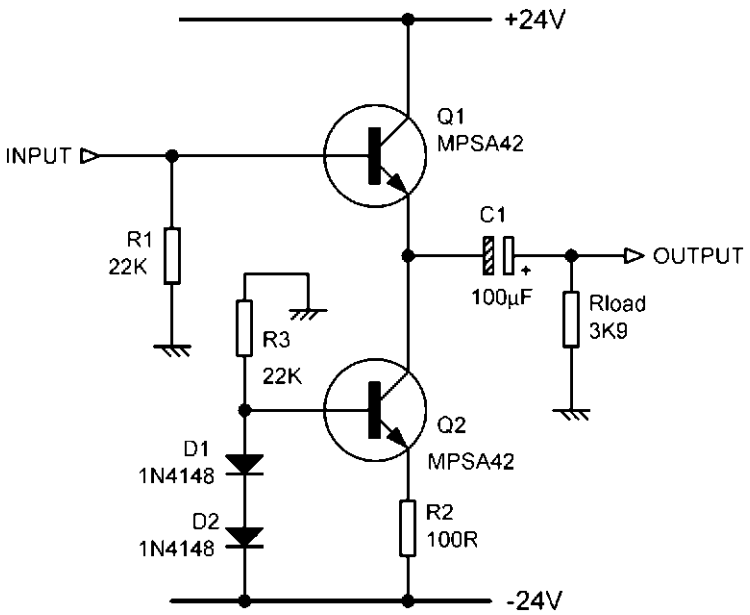

Figure 3.5: Emitter-follower with a constant-current source replacing the emitter resistor

The 22 kΩ resistor R3 in turn biases the diodes. This simple bias system works quite adequately if the supply rails are regulated, but might require filtering if they are not. The 22 kΩ value is non-critical; so long as the diode current exceeds the I_b of Q2 by a reasonable factor (say 10 times) there will be no problem.

Figure 3.6 shows that distortion is much reduced. With no external load, 0.013% at 4 Vrms has become less than 0.0003%, the measurement system noise floor. This is because the amount by which the collector current is modulated is very much reduced. The linearity of this emitter-follower is still degraded by increasing loading, but to a much lesser extent; with a significant external load of 4k7, 0.036% at 4 Vrms becomes 0.006%. The steps in the bottom (no load) trace are artefacts of the AP SYS-2702 measuring system.

The noise performance of this stage is exactly as for the simple emitter-follower above.

The Push–Pull Emitter-Follower

This is an extremely useful and trouble-free form of push–pull output; I have used it many times in preamplifiers, mixers, etc. I derived the notion from the valve-technology White cathode-follower, described by Nelson-Jones in a long-ago *Wireless World* [7]. The original reference is a British patent taken out by Eric White in 1940 [8].

Figure 3.7 shows a push–pull emitter-follower. When the output is sourcing current, there is a voltage drop through the upper sensing resistor R5, so its lower end goes downwards in

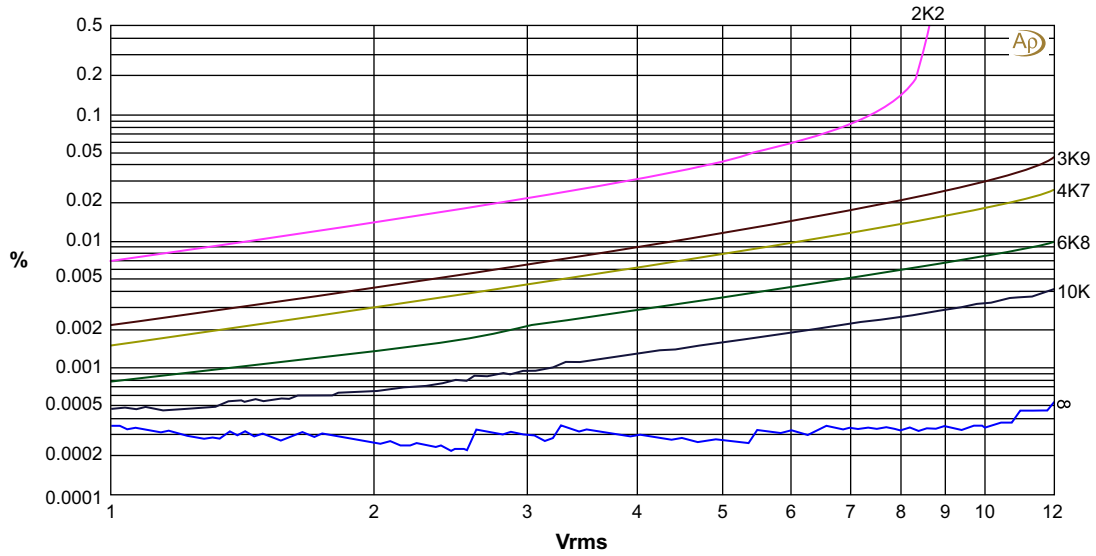

Figure 3.6: How various loads degrade the linearity of the current-source emitter-follower. The quiescent current was 6 mA

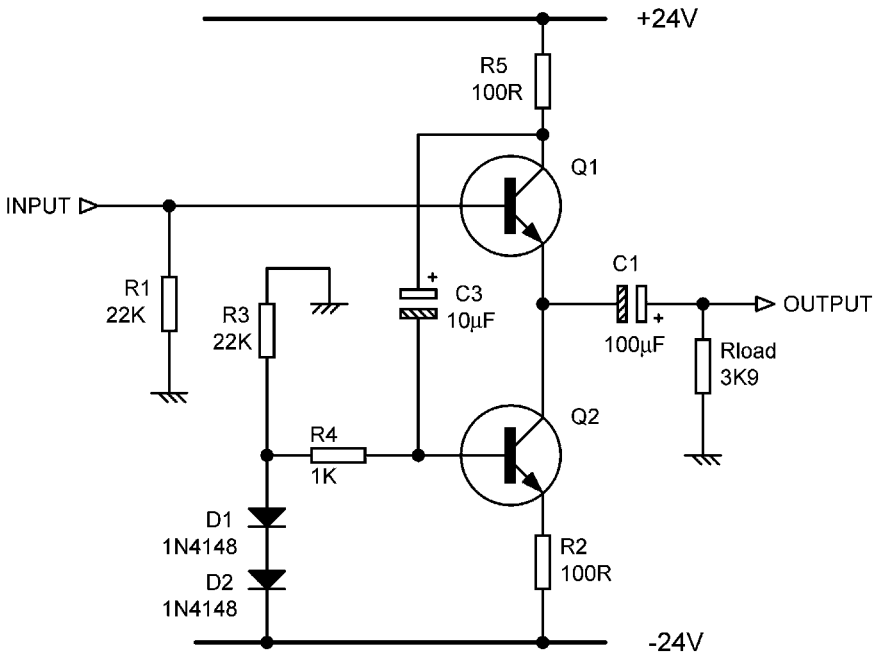

Figure 3.7: Circuit of push–pull emitter-follower. Quiescent current still 6 mA as before, but the load-driving capability is twice as great

voltage. This is coupled to the current source Q2 through C3, and tends to turn it off. Likewise, when the current through Q1 falls, Q2 is turned on more. This is essentially a negative-feedback loop with an open-loop gain of unity, and so by simple arithmetic the current variations in Q1, Q2 are halved, and this stage can sink twice the current of the constant-current version described above, while running at the same quiescent current. The effect of loading on linearity is once again considerably reduced, and only one resistor and one capacitor have been added.

This configuration needs fairly clean supply rails to work, as any upper-rail ripple or disturbance is passed directly through C3 to the current source, modulating the quiescent current and disrupting the operation of the circuit.

Push–pull action further improves the linearity of load driving; the THD with a 4k7 external load is halved, from 0.006% at 4 Vrms to 0.003%, at the same quiescent current of 6 mA, as seen in Figure 3.8. This is pretty good linearity for such simple circuitry.

Emitter-Follower Stability

The emitter-follower is about as simple as an amplifier gets, and it seems highly unlikely that it could suffer from obscure stability problems. However, it can, and often does. Emitter-followers

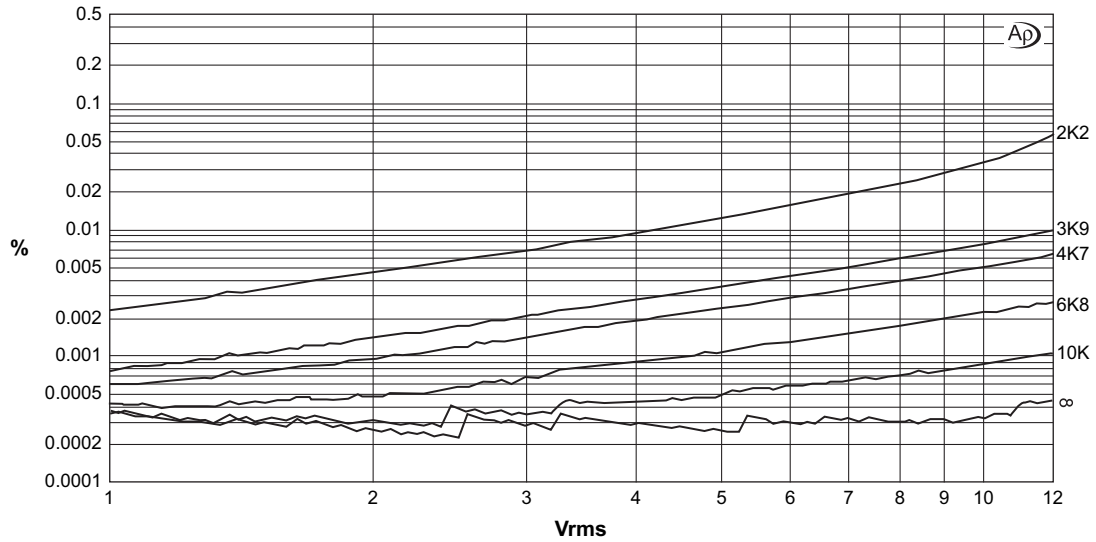

Figure 3.8: How loading degrades linearity of the push–pull emitter-follower. Loads from 10 kΩ to 2k2

are liable to RF oscillation when fed from inductive source impedances. This oscillation is in the VHF region, usually in the area 100–400 MHz, and will be quite invisible on the average oscilloscope; however, a sure sign of this problem is unusually high distortion that varies strongly when the transistor is touched with a probing finger. One way to stop this is to put a 'base-stopper' resistor directly in series with the base. This should come after the bias resistor to prevent loss of gain. Depending on the circuit conditions, the resistor may be as low as 100 Ω or as high as 2k7. The latter generates −119.6 dBu of Johnson noise, which in itself is inconvenient in low-noise circuitry, but the effects of the transistor noise current flowing through it are likely to be even worse. Base-stopper resistors are not shown in the following diagrams to aid clarity, but you should always be aware of the possible need for them. This also applies to the CFP configuration, which is equally, if not more, susceptible to the problem.

The instability is due to the fact that the typical emitter-follower is fed from a source with some inductance, and has some capacitive loading, even if it is only due to stray capacitance, as in Figure 3.9(a), where the transistor internal base-emitter capacitance C_{be} is included. If this is redrawn as in Figure 3.9(b), it is the classic circuit of a Colpitts oscillator.

For more information on this phenomenon, see Feucht [9] and de Lange [10].

CFP Emitter-Followers

The simple emitter-follower is lacking both in linearity and load-driving ability. The first shortcoming can be addressed by adding a second transistor to increase the negative-feedback

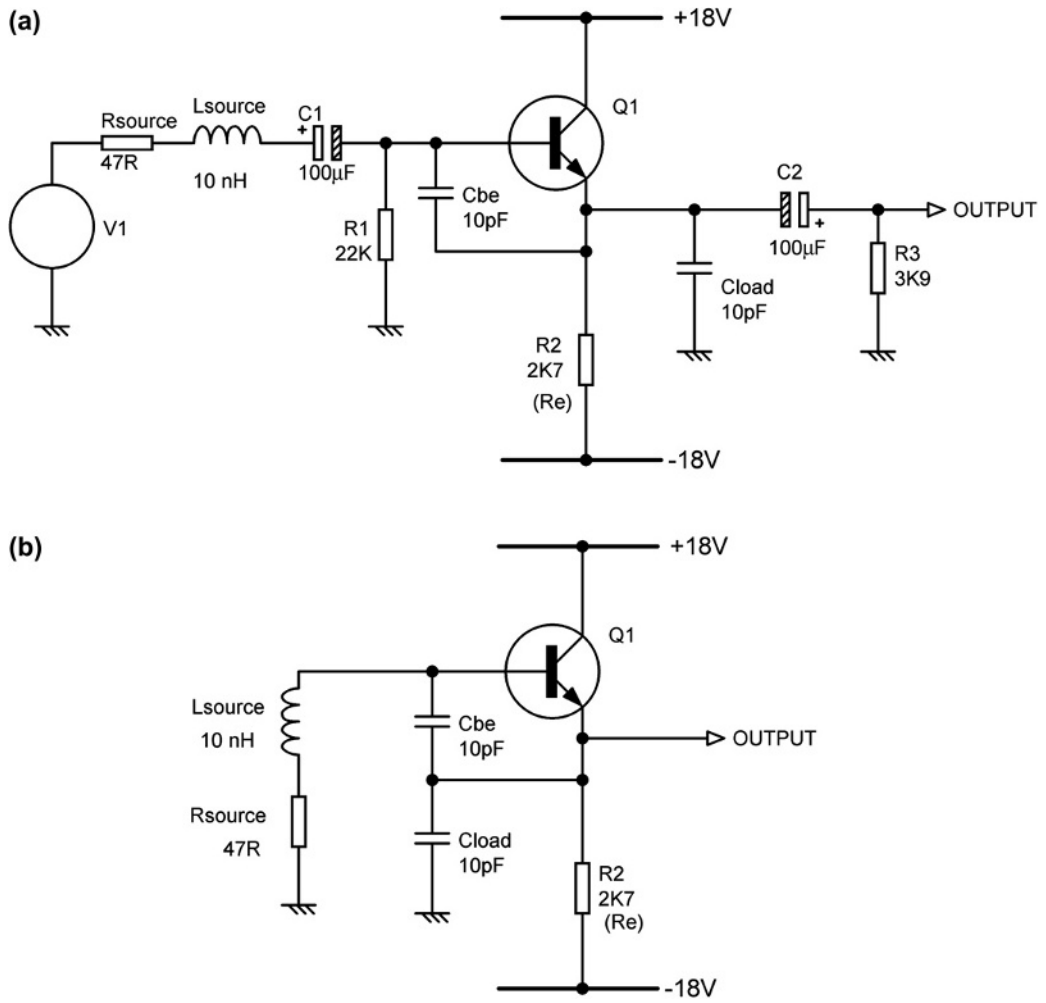

Figure 3.9: Emitter-follower oscillation: the effective circuit at (a) bears a startling resemblance to the Colpitts oscillator at (b)

factor by increasing the open-loop gain. This also allows the stage to be configured to give voltage gain, as the output and feedback point are no longer inherently the same. This arrangement is usually called the complementary feedback pair (CFP), though it is sometimes known as the Szilaki configuration. This circuit can be modified for constant-current or push–pull operation exactly as for the simple emitter-follower.

Figure 3.10 shows an example. The emitter resistor Re is the same value as in the simple emitter-follower to allow meaningful comparisons. The value of R4 is crucial to good linearity, as it sets the I_c of the first transistor, and determines its collector loading. The value of 3k3 shown here is a good compromise.

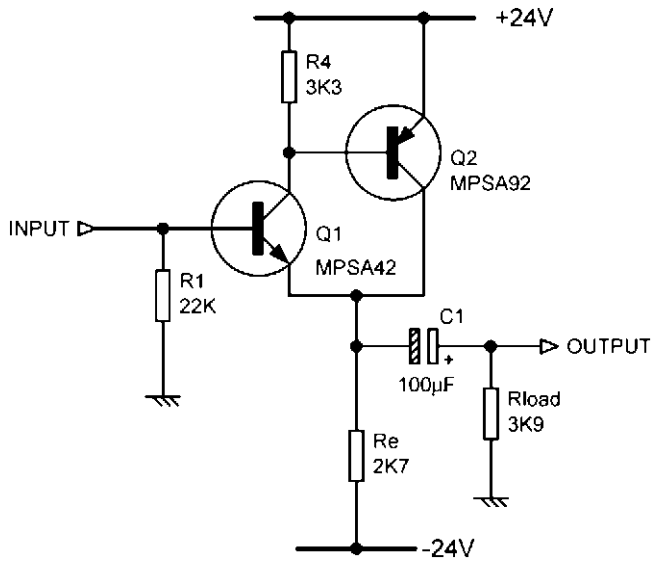

Figure 3.10: The CFP emitter-follower. The single transistor is replaced by a pair with 100% voltage feedback to the emitter of the first transistor

This circuit is also susceptible to emitter-follower oscillation, particularly if it sees some load capacitance, and will probably need a base stopper. If 1 kΩ does not do the job, try adding a series output resistor of 100 Ω close to the stage to isolate it from load capacitance.

Figure 3.11 shows the improved linearity; Figure 3.12 is the corresponding SPICE simulation. The measured noise output with a 100 Ω base stopper is −116.1 dBu.

If we replace Re with a 6 mA current source, as in Figure 3.13, we once more get improved linearity and load-driving capability, as shown in Figure 3.14. The 6 Vrms, 6k8 THD is now only just above the noise at 0.0005% (yes, three zeros after the point: three-transistor circuitry can be rather effective).

Converting the constant-current CFP to push–pull operation as in Figure 3.15 gives another improvement in linearity and load driving. Figure 3.16 shows that now only the results for 2k2 and 3k9 loading are above the measurement floor.

Improved Unity-Gain Buffers

There is often a need for a unity-gain buffer with very low distortion. If neither the simple emitter-follower, made with one transistor, nor the CFP configuration with two transistors is adequately linear, we might ponder the advantages of adding a third transistor to improve performance, without going to the complexity of the discrete op-amps described later in this chapter. (In our transistor count we are ignoring current sources used to create the active output loads that so improve linearity into significant external loading.)

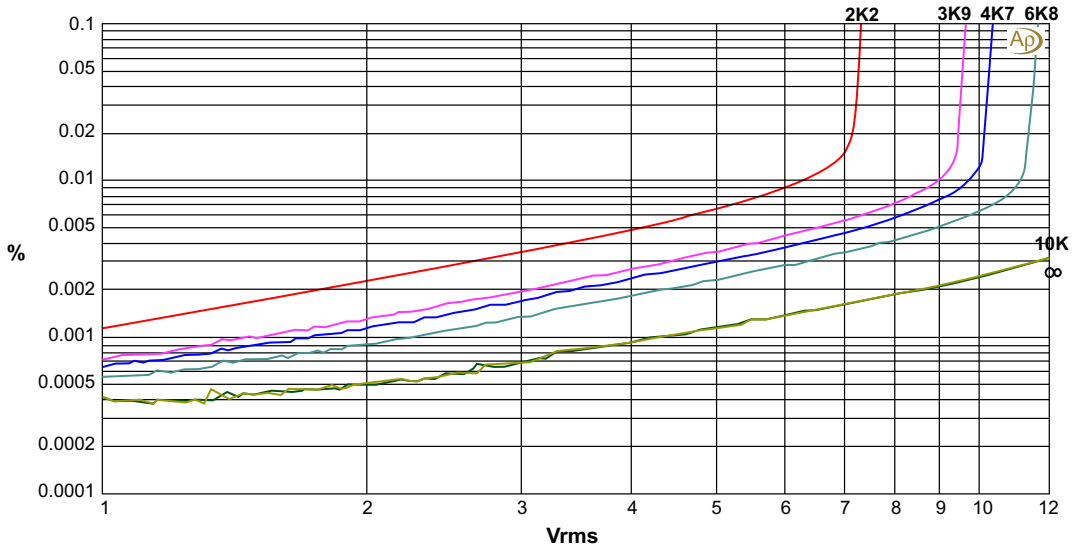

Figure 3.11: How loading affects the distortion of a CFP emitter-follower. THD at 6 Vrms, 6k8 load is only 0.003% compared with 0.05% for the simple EF. Re is 2k7

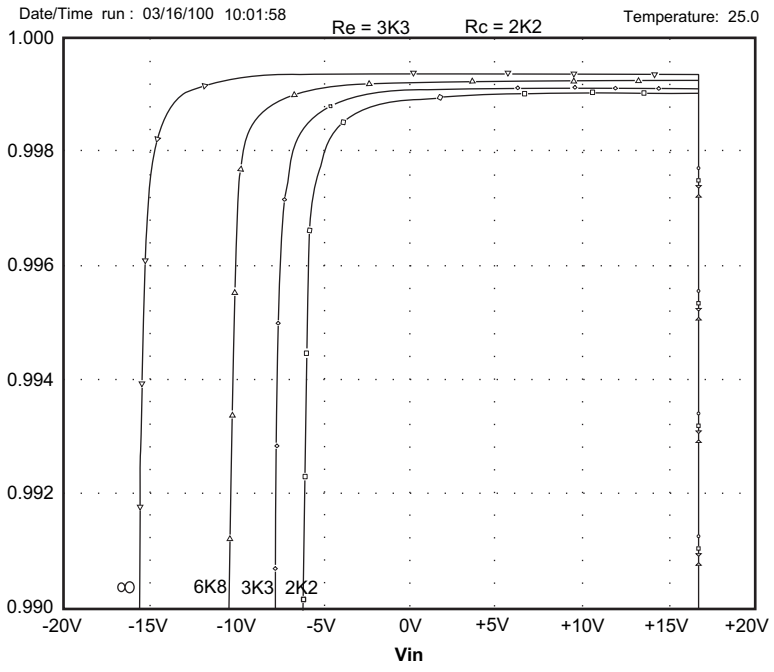

Figure 3.12: SPICE simulation of the circuit in Figure 3.10, for different load resistances. The curves are much flatter than those in Figure 3.4, even though the vertical scale has been expanded

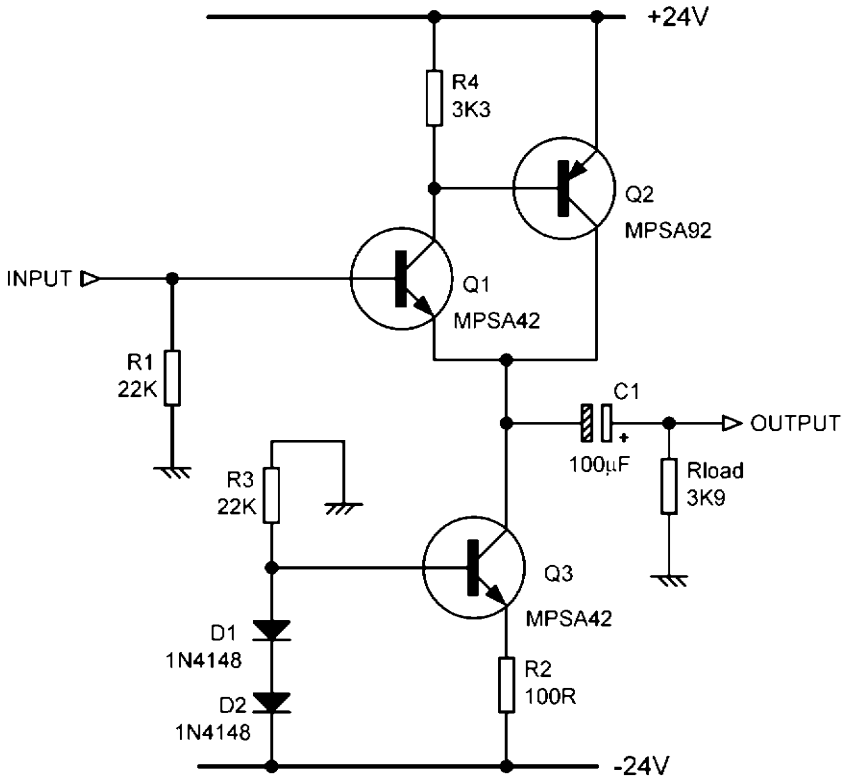

Figure 3.13: Constant-current CFP follower. Once more the resistive emitter load is replaced by a constant-current source to improve current sinking

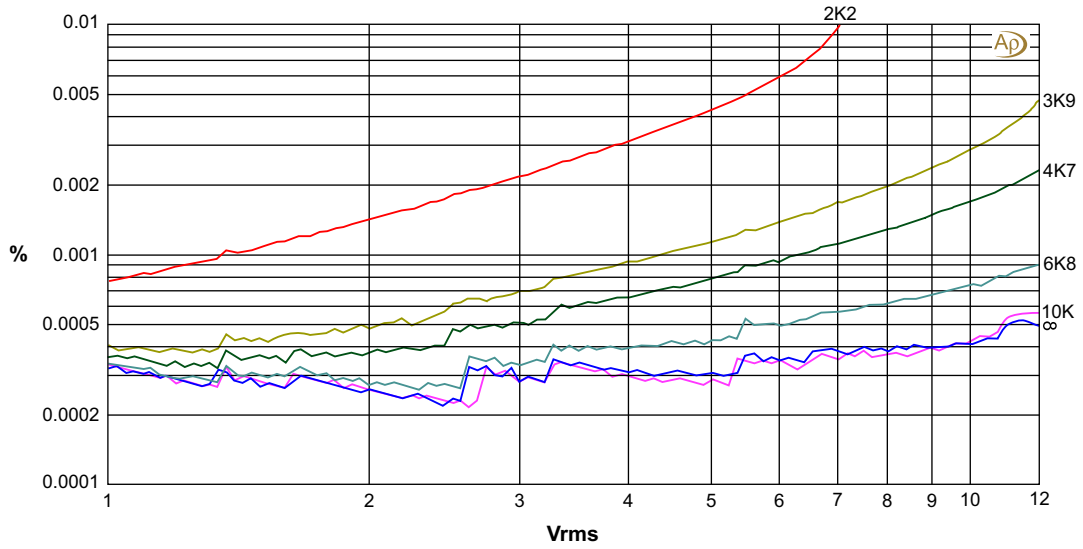

Figure 3.14: Distortion and loading effects on the CFP emitter-follower with a 6 mA current source. The steps on the lower traces are artefacts caused by the measurement system gain-ranging as it attempts to measure the THD of pure noise. Note change of scale

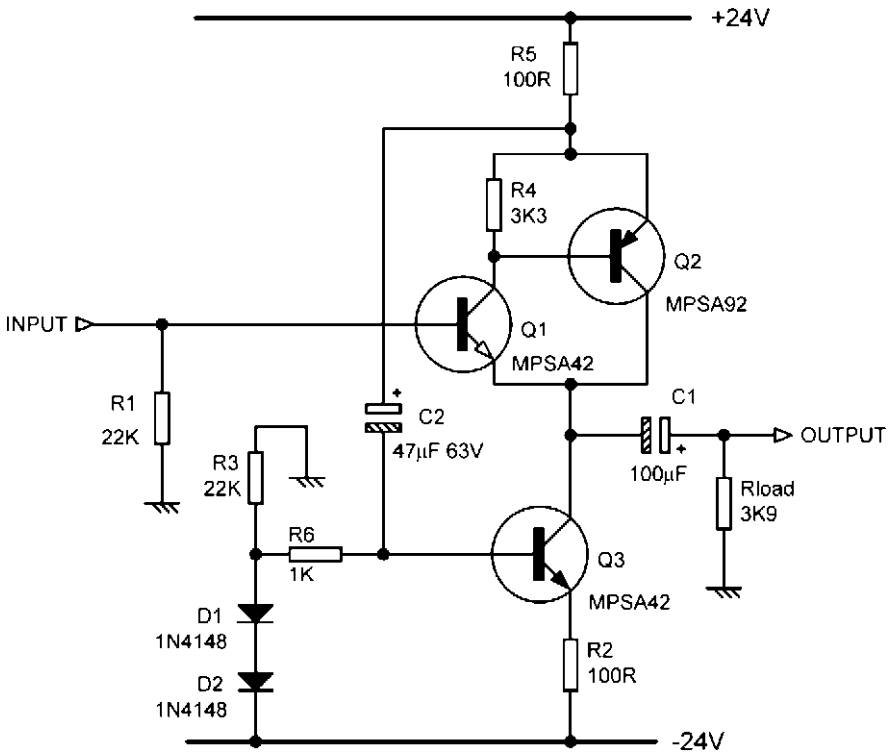

Figure 3.15: Circuit of a push–pull CFP follower. This version once more gives twice the load-driving capability for no increase in standing current

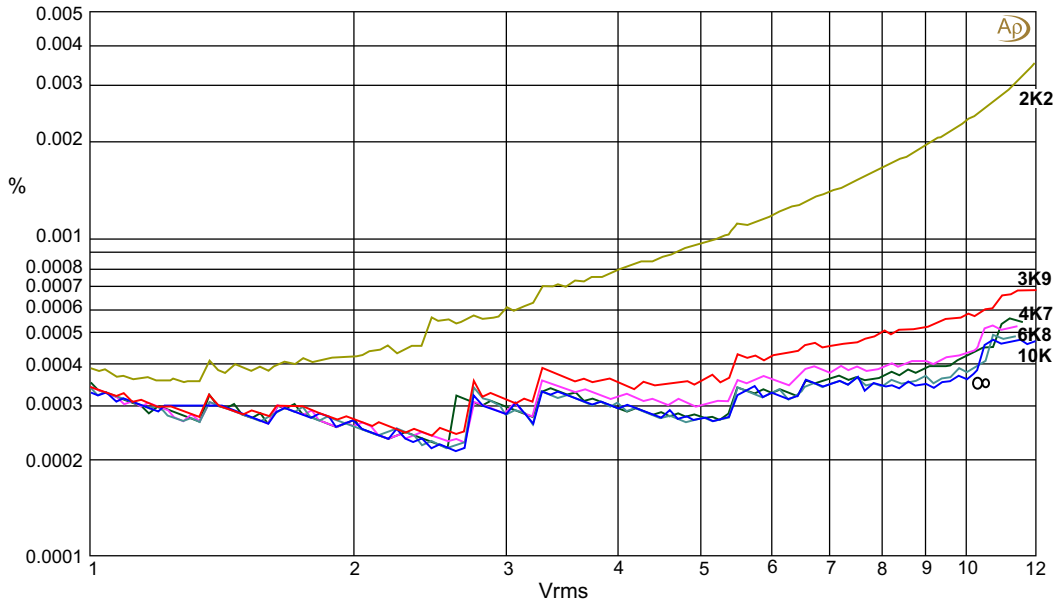

Figure 3.16: Distortion and loading effects on the push–pull CFP emitter-follower, still with 6 mA of quiescent current

One promising next step is a three-transistor configuration that is often called the Schlotzaur configuration (see Feucht [5] and Staric and Margan [11]). The single input transistor in the CFP emitter-follower is now replaced with a long-tail pair with 100% feedback to Q2, as in Figure 3.17(a). Because long-tail pair have the property of canceling out their even-order distortion [6], you might expect a considerable improvement. You would be wrong; running on ±15 V rails we get 0.014% at 6 Vrms unloaded, almost flat across the audio band. The linearity is much inferior to the CFP emitter-follower. The open-loop gain, determined by measuring the error voltage between Q1, Q2 bases, is 249 times.

It's not a promising start, but we will persist! Replace the collector load R2 with a current source of half the value of the tail current source as in Figure 3.17(b) and the linearity is transformed, yielding 0.00075% at 6 Vrms unloaded on ±15 V rails. Increasing the rails to ±18 V gives 0.00066% at 6 Vrms; and a further increase to ±24 V, as high-voltage operation is part of what discrete design is all about, gives 0.00042% at 6 Vrms (unloaded). It's the increase in the positive rail that gives the improvement. Reducing the measurement bandwidth from 80 to 22 kHz for a 1 kHz signal eliminates some noise and gives a truer figure of 0.00032% at 6 Vrms. The open-loop gain is increased to 3400 times.

Adding loading to the buffer actually has very little effect on the linearity, but its output capability is clearly limited by the use of R3 to sink current, just as for a simple emitter-follower. Replacing R3 with a 6 mA constant-current source, as for previous circuits, much improves drive capability and also improves linearity somewhat (see Figure 3.17(c)). On ±30 V rails we get a reading of 0.00019% at 5 Vrms with a 2k2 load, and that is mostly the noise in a 22 kHz bandwidth.

Finally we remove current source I2 and replace it with a simple current mirror in the input pair collectors, as in Figure 3.17(d), in the pious hope that the open-loop gain will be doubled and distortion halved. On ±30 V rails there is a drop in THD from 0.00019% to 0.00017% at 5 Vrms with a 2k2 load (22 kHz bandwidth), but that is almost all noise and I am pushing the limits of even the magnificent Audio Precision SYS-2702. This goes to show that there are other ways of designing low-distortion circuitry apart from hefting a bucket of 5532s.

Figure 3.18 shows the distortion plot at 5 Vrms. Using an 80 kHz bandwidth so the HF end is meaningful means the readings are higher, and virtually all noise below 10 kHz. It also gives another illustration of the distortion generated by undersized coupling capacitors. C1 started as 22 µF, but you can see that 220 µF is required to eliminate distortion at 10 Hz with a 2k2 load.

SPICE analysis shows that the collector currents of the input pair Q1, Q2 are somewhat unbalanced by the familiar base-current errors of a simple current mirror. Replacing the simple current mirror with the well-known Wilson improved mirror might get us further improvement, if we could measure it. Work in progress …

The circuit we have now could still be regarded as a much-enhanced emitter-follower, but it is probably more realistic to consider it as a two-stage discrete op-amp.

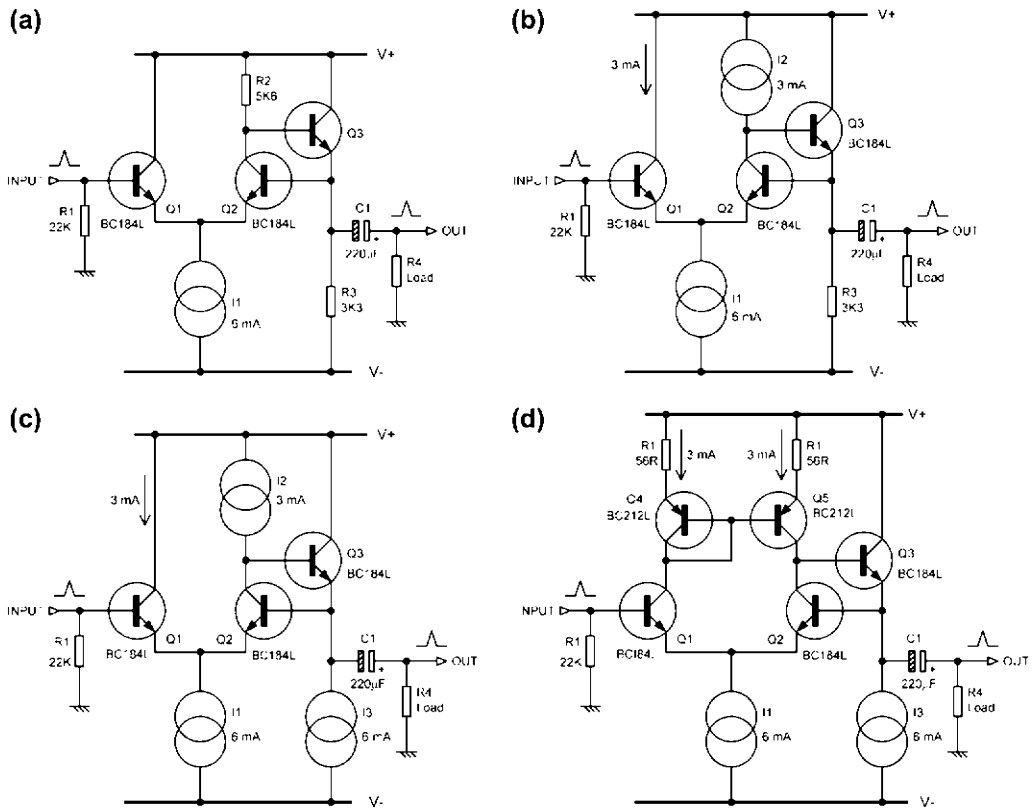

Figure 3.17: Developing a unity-gain buffer design, which replaces the single input transistor with a long-tailed pair. (a) Simple Schlotzaur circuit. (b) Collector load R2 replaced with current source. (c) Output current source added. (d) Inserting current mirror in input pair collectors

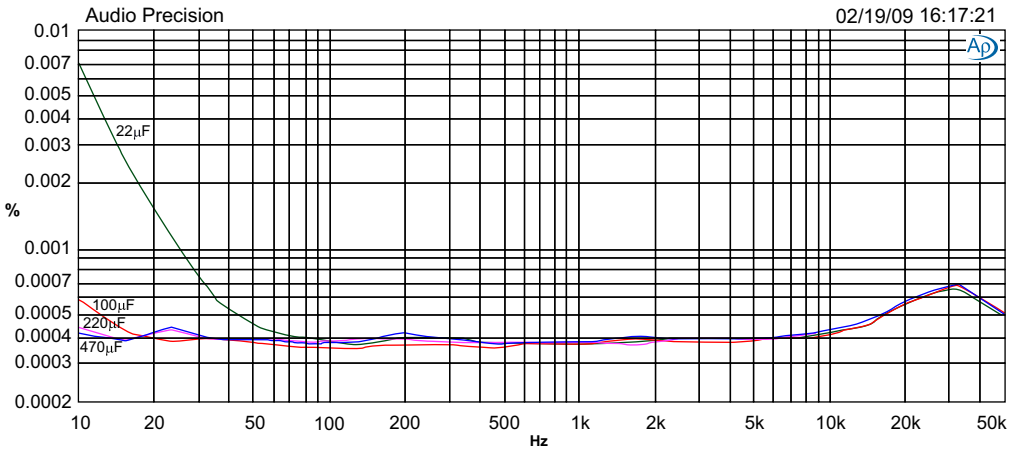

Figure 3.18: THD plot for the final version of the buffer, at 5 Vrms with a 2k2 load. The rising LF curves illustrate the distortion generated by undersized output capacitors. Bandwidth 80 kHz

Gain Stages

This section covers any discrete transistor stage that can give voltage gain. It may be as simple as a single transistor or as complex as an op-amp implemented with discrete components. A single transistor can give voltage gain in either series or shunt mode.

One-Transistor Shunt-Feedback Gain Stages

Single-transistor shunt-feedback gain stages are inherently inverting, and of very poor linearity by modern standards. The circuit in Figure 3.19 is inevitably a collection of compromises. The collector resistor R4 should be high in value to maximize the open-loop gain, but this reduces the collector current of Q1, and thus its transconductance, and hence reduces open-loop gain once more. The collector resistor must also be reasonably low in value as the collector must drive external loads directly. Resistor R2, in conjunction with R3, sets the operating conditions. This stage has only a modest amount of shunt feedback via R3, and the input can hardly be called a virtual earth. However, such circuits were once very common in low-end discrete preamplifiers, back in the days when the cost of an active device was a serious matter. Such stages are still occasionally found doing humble jobs like driving VU meters, but the cost advantage over an op-amp section is small, if it exists at all.

The gain of the stage in Figure 3.19 is at a first look 220k/68k = 3.23 times, but the actual gain is 2.3× (with no load) due to the small amount of open-loop gain available. The mediocre distortion performance that must be expected even with this low gain is shown in Figure 3.20.

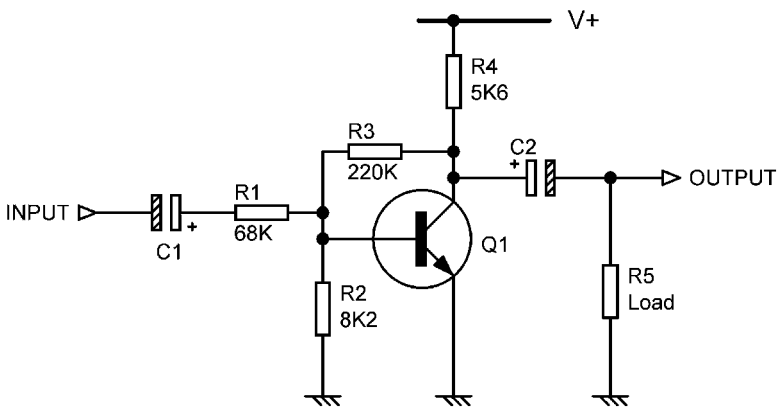

Figure 3.19: Circuit of single-transistor gain stage, shunt-feedback version

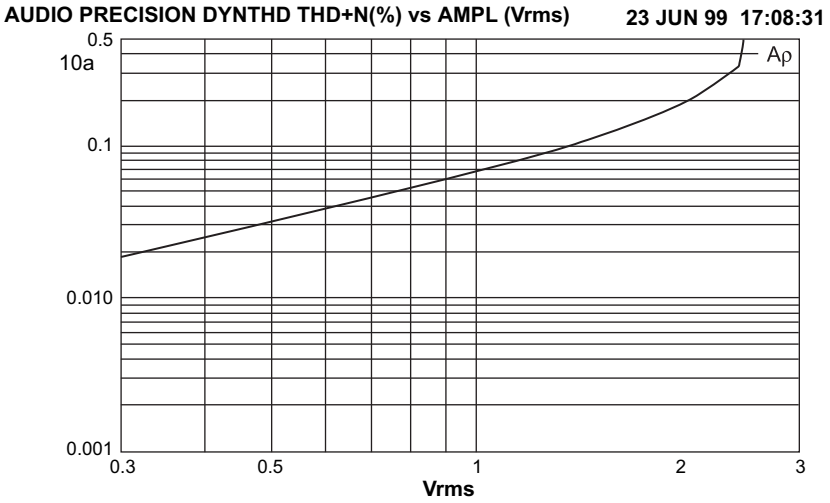

Figure 3.20: Single-transistor shunt-feedback gain stage, distortion versus level. Gain is 2.3 times

One-Transistor Series-Feedback Gain Stages

Single-transistor series-feedback gain stages are made by creating a common-emitter amplifier with a feedback resistor that gives series voltage feedback to the emitter. The gain is the ratio of the collector and emitter resistors, if loading is negligible. Note that unlike op-amp-based series-feedback stages, this one is inherently inverting. To make a non-inverting stage with a gain more than unity requires at least two transistors, because of the inversion in a single common-emitter stage.

This very simple stage, shown in Figure 3.21, naturally has disadvantages. The output impedance is high, being essentially the value of the collector resistor R3. The output is neither good at sinking nor sourcing current.

The distortion performance as seen in Figure 3.22 is indifferent, giving 0.3% THD at 1 Vrms out. Compare this with the shunt-feedback one-transistor gain stage above, which gives 0.07% under similar conditions.

Two-Transistor Shunt-Feedback Gain Stages

Before the advent of the op-amp, inverting stages were required for tone controls and virtual-earth summing amplifiers. The one-transistor amplifier stage already described is deficient in distortion and load-driving capability. See Figure 3.24 for distortion performance. A much better amplifier can be made with two transistors, as in Figure 3.23. The voltage gain is generated by Q1, which has a much higher collector resistor R4 and so much higher gain. This is possible because Q2 buffers it from external loading, and allows a higher NFB factor.

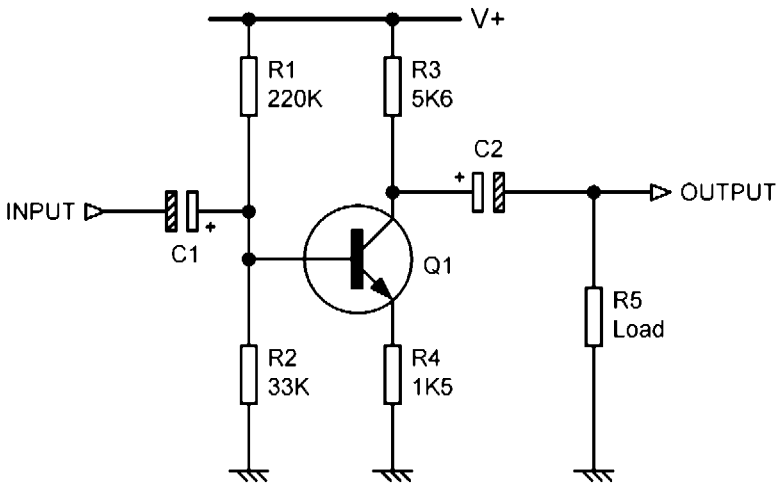

Figure 3.21: Circuit of single-transistor series-feedback gain stage

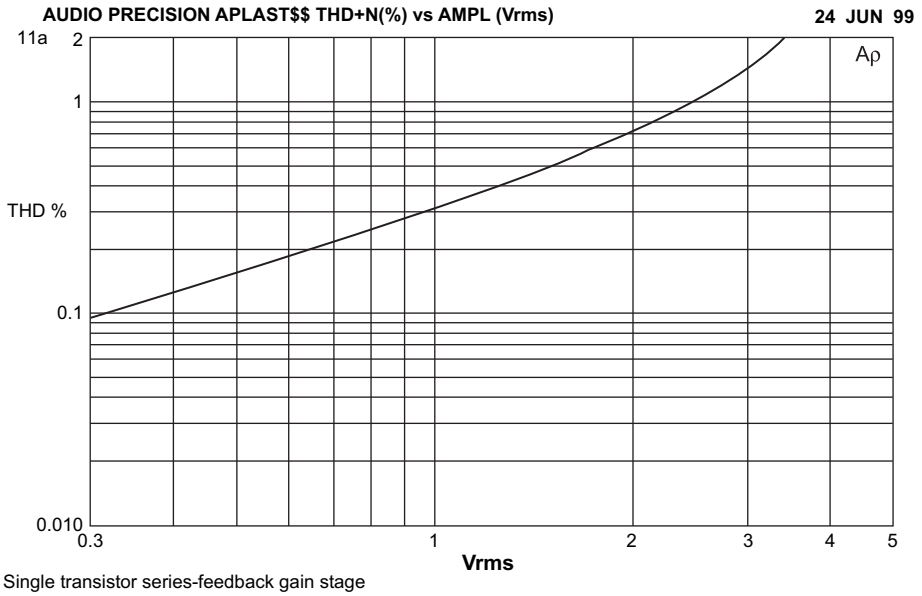

Figure 3.22: Single-transistor series-feedback gain stage, distortion versus input level. Gain is 3

With the addition of bootstrapping, as shown in Figure 3.25, the two-transistor stage has its performance transformed. Figure 3.26 shows how THD is reduced by a factor of 10; 0.15% at 1 Vrms in, 3 Vrms out becomes 0.015%, which is much more respectable. The improvement is due to the increased voltage gain of the first stage, giving a higher NFB factor. THD is still approximately proportional to level, as the distortion products are mainly second harmonic.

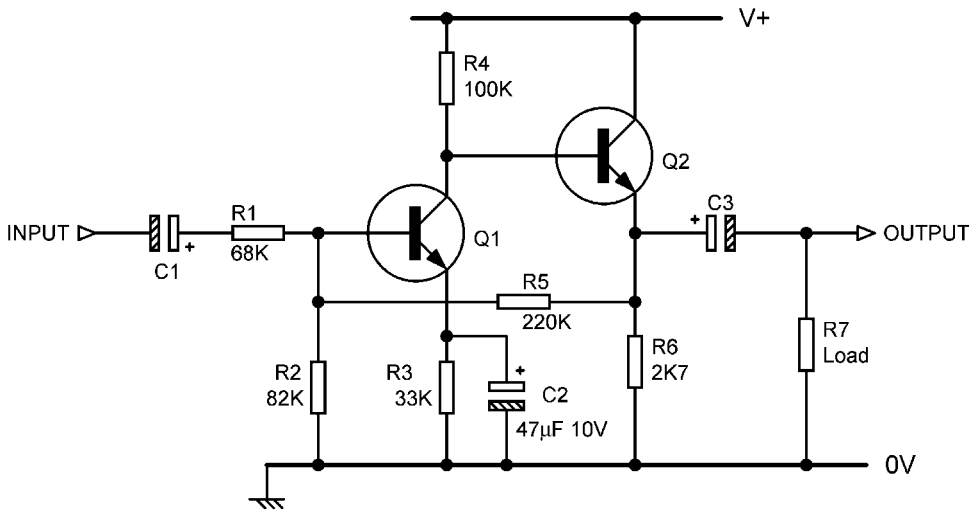

Figure 3.23: Two-transistor gain stage with shunt-feedback. Gain is 3

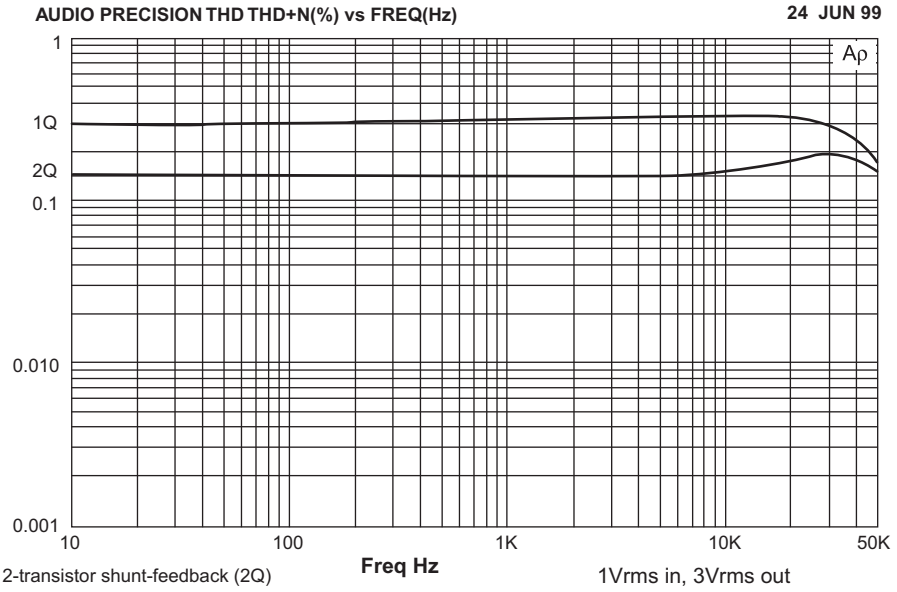

Figure 3.24: Distortion of two-transistor shunt stage versus frequency (2Q). Distortion of the one-transistor version (1Q) is also shown. The two-transistor version is only twice as good, which seems a poor return for the extra active device

Clipping occurs abruptly at 2.9 Vrms in, 8.7 Vrms out; abrupt clipping onset is characteristic of stages with a high NFB factor.

Stages like this were commonly used as virtual-earth summing amplifiers in mixing consoles before acceptable op-amps were available at reasonable cost.

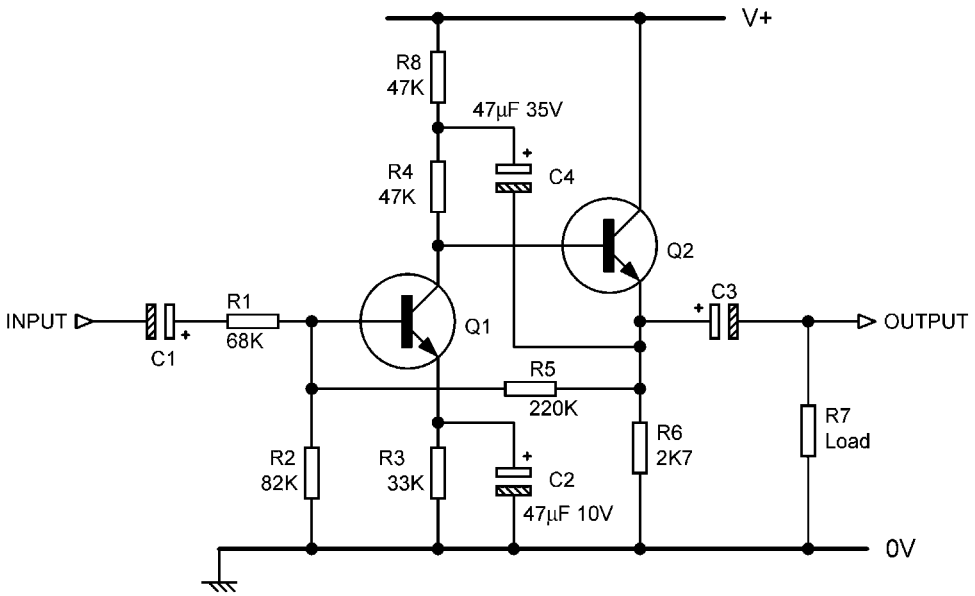

Figure 3.25: Two-transistor shunt-feedback stage, with bootstrapping added to the first stage to improve linearity

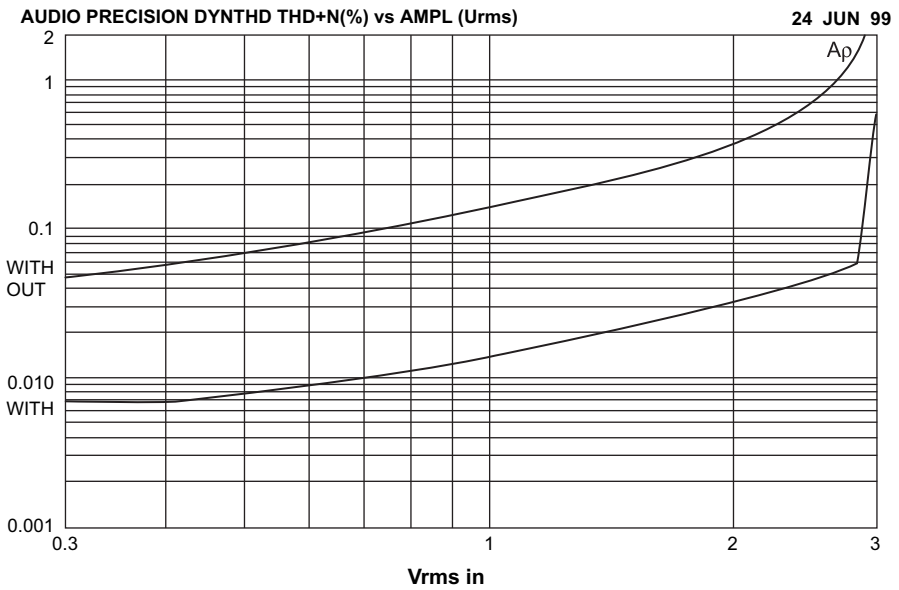

Figure 3.26: Distortion of the two-transistor shunt stage versus level, with and without bootstrapping. *X*-axis is input level; output is three times this

Figure 3.27 shows that the distortion is further reduced to 0.002% at 3 Vrms out if the impedance of the input and feedback networks is reduced by 10 times. SPICE simulation confirms that this is because the signal currents flowing in R1 and R5 are now larger compared with the non-linear currents drawn by the base of Q1. There is also a noise advantage.

Increasing the supply reduces the distortion for a given output level in this kind of stage. A version with the low-impedance feedback values gave 0.0044% at 1 kHz for a 3 Vrms output with a +24V rail; increasing the supply voltage to +30V reduced this to 0.0032%, while +40V gave 0.0023%. The biasing system adjusts itself to these changes. A creditable performance for such a simple circuit.

Distortion can also be improved by tweaking the value of the emitter-follower load R6, to partially cancel the curvatures of the first and second stages. With a +24V rail and R6 at 2k7 as shown, THD is 0.0044% at 3 Vrms out, but reducing R6 to 2k2 drops the distortion to 0.0038%, while 2k0 gives 0.0035%. The latter figure is 79% lower, the only cost being a slight increase in power consumption.

Another important point is that the bootstrap capacitor needs to be larger than you might think. Reducing it to 2.2 µF here gives rising distortion at LF, with a ten-fold increase at 10 Hz. This is because the gain increase given by bootstrapping is very sensitive to the AC voltage at the top of the capacitor.

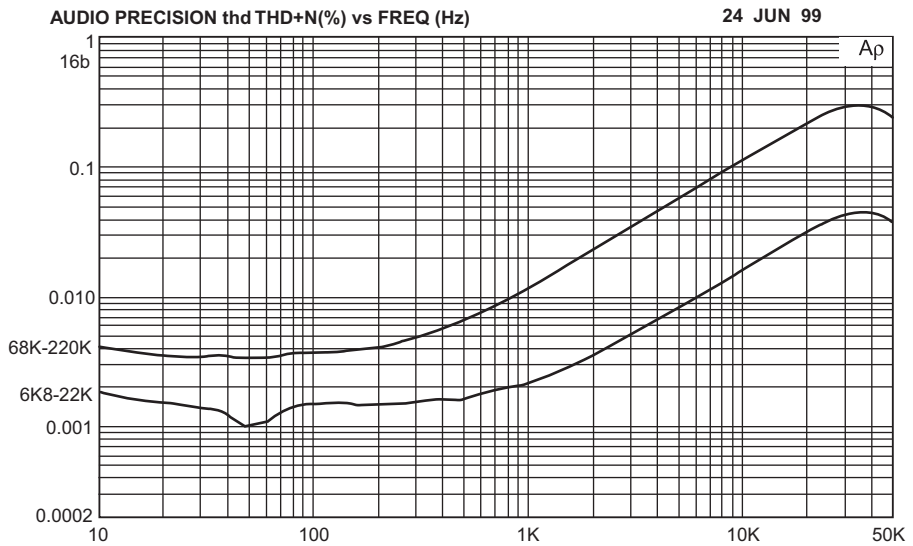

Figure 3.27: The distortion is reduced by a further factor of at least 5 if the impedance of the input and feedback networks is reduced by 10 times. Output 3 Vrms

Figure 3.28 shows how output drive capability can be increased, as before, by replacing R6 with a 6 mA current source. The input and feedback resistors R1, R5 have again been scaled down by a factor of 10. Push–pull operation can also be simply implemented as before. The EIN of this version is -116 dBu.

The constant-current and push–pull options can also be added to more complex discrete stages. Some good examples can be found in a preamplifier design of mine [12].

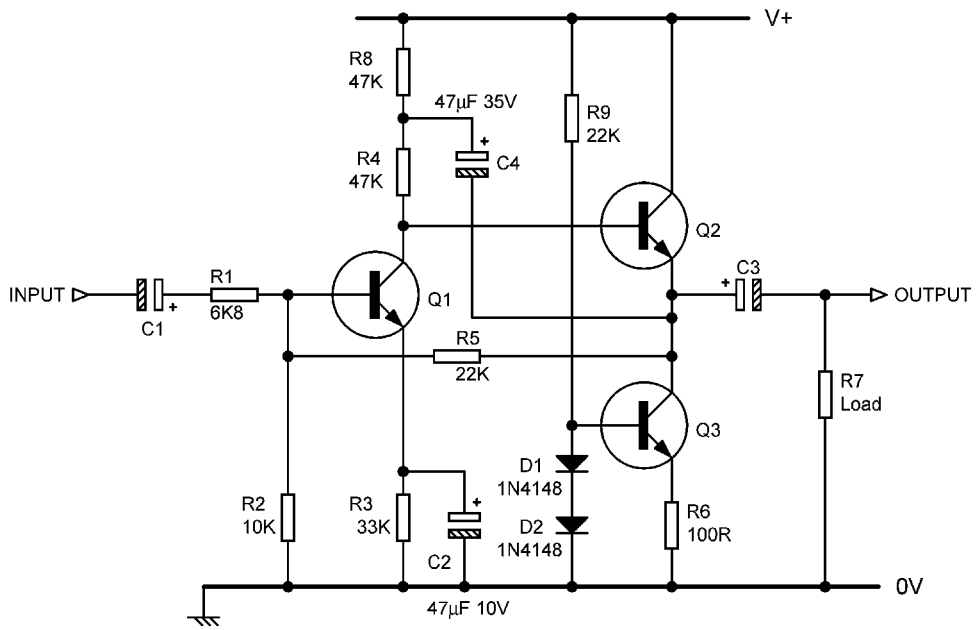

Figure 3.28: Two-transistor bootstrapped shunt-feedback stage, with low-impedance feedback network, and with current-source output to enhance load-driving capability

Two-Transistor Series-Feedback Gain Stages

This circuit clearly has a close family relationship with the CFP emitter-follower, which is simply one of these stages configured for unity gain. The crucial difference here is that the output is separated from the input emitter, so the closed-loop gain is set by the R3–R2 divider ratio. See Figure 3.29.

Only limited NFB is available, so closed-loop gains of two or three times are usually the limit. It is less easy to adapt this circuit to improve load-driving capability, because the feedback resistive divider must be retained. Figure 3.30 shows that distortion performance depends strongly on the value of R4, the collector load for Q1. The optimal value for linearity and noise performance is around 4k7.

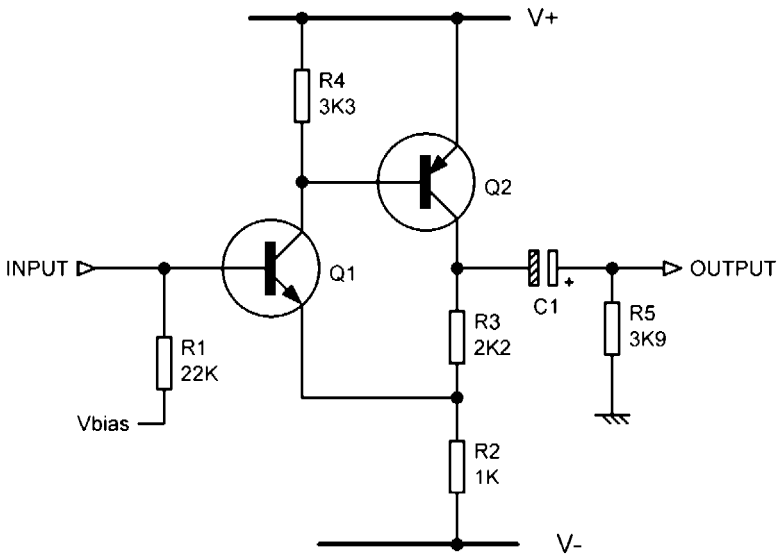

Figure 3.29: Two-transistor gain stage, series feedback. Gain once more is approximately 3

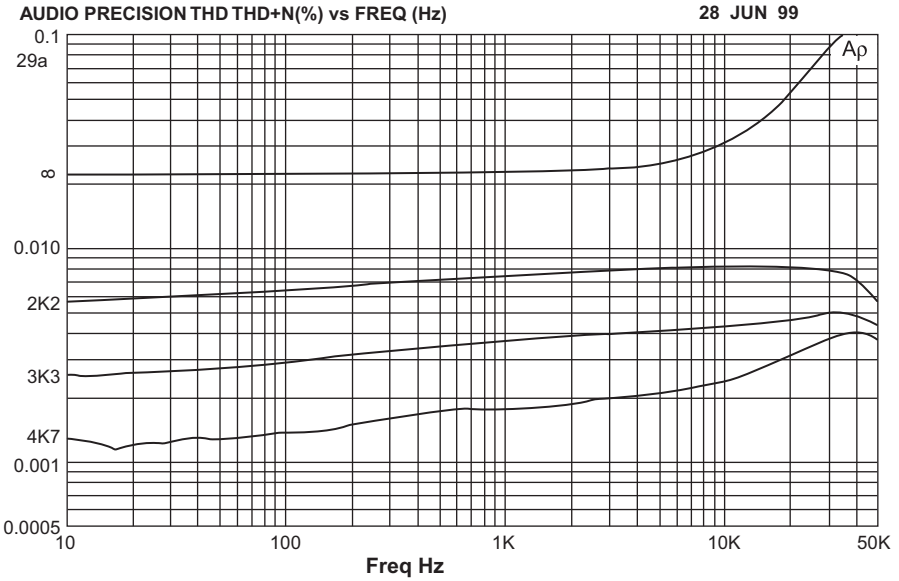

Figure 3.30: Two-transistor series-feedback stage. THD varies strongly with value of R4

Discrete Op-Amp Design

When the previously described circuits do not show enough linearity or precision for the job in hand, or a true differential input is required, it may be time to turn to op-amp design using discrete transistors. This section does not pretend to be an exhaustive guide, but

concentrates on audio issues such as distortion. Much that can be found in standard op-amp textbooks is taken for granted. It does, however, give information that I do not think appears anywhere else.

The op-amp in Figure 3.31 is conventional in design; its resemblance to a power amplifier circuit is obvious. It consists of three stages: the differential input stage Q1–Q3, the voltage-amplifier stage (VAS) Q4, Q5, and a unity-gain output stage Q7, Q8.

The long-tailed pair first stage Q2, Q3 subtracts the input and feedback voltages; it is a transconductance amplifier, i.e. it turns a voltage input into a current output. The voltage/current gain curve of this stage peaks at the center, where the collector currents of Q2, Q3 are equal, and is its most linear part. As a result the value of R2 is crucial; if the I_c values are unbalanced there is a wholly avoidable rise in second-harmonic THD at high frequencies. Since global NFB establishes 0.6 V across R2, simply making it equal to R3 does not do the job; it needs to be approximately equal to half the value of the resistor R1 that sets the tail current. This is demonstrated in Figure 3.32.

This rapid rise in first-stage distortion with frequency is because:

- at high frequencies more current flows in and out of the dominant-pole capacitor C3. At the input side of the capacitor this can only be provided by the input stage, which has to work harder – in other words, the error voltage is greater so the output current has a larger swing over more of the transfer characteristic;

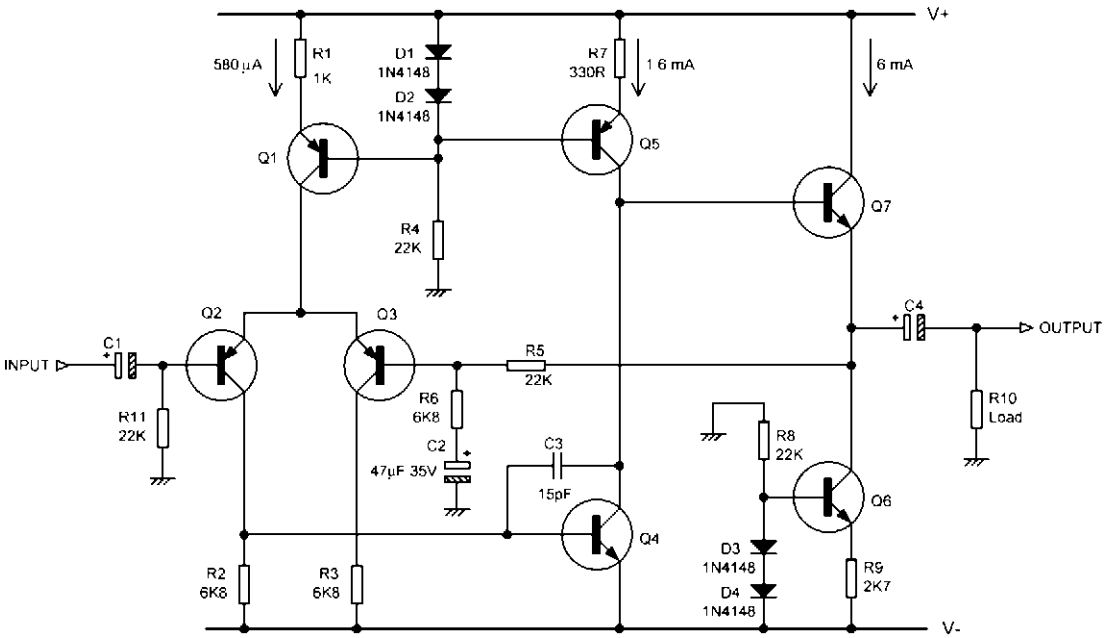

Figure 3.31: A typical discrete op-amp circuit, with current-source output

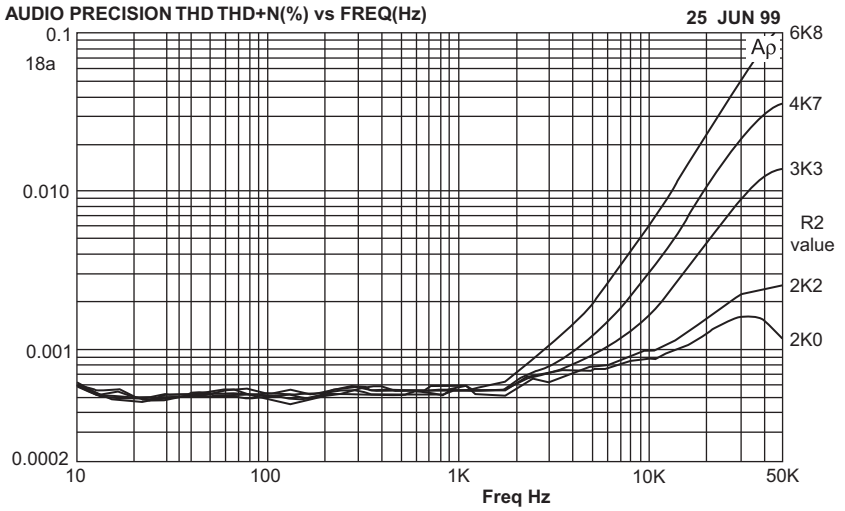

Figure 3.32: Reduction in high-frequency THD as input stage approaches balance with R2 = 2 kΩ

- once the input stage is balanced, it creates only third-harmonic distortion, which rises as the square of LTP input voltage;
- there is less global NFB at high frequencies due to C3.

The first-stage output current flows into the second voltage-amplifier stage Q4, Q5. This is a transadmittance amplifier; current in becomes voltage out. The input is at low impedance (a sort of virtual earth) because of local NFB through dominant-pole capacitor C3, and so is well adapted to accepting the output current from the first stage.

The third stage is a unity-gain buffer, isolating the VAS collector from external loads. The higher the quiescent current in this stage (here 6 mA as before), the lower the load impedance that can be driven symmetrically.

An improved circuit is shown in Figure 3.33. R2 has been given its correct value; R3 has now been altered to match but this change is purely cosmetic. The distortion performance is shown in Figure 3.34. Much more information on LTP input stage design can be found in Chapter 4 of Ref. [6].

The operating conditions of the op-amp are set by the three currents shown in the figures. The tail current of the first stage is probably the most critical, as this sets:

- the transconductance of the input pair. This in turn affects the open-loop gain of the amplifier and therefore stability when the loop is closed;
- the maximum output slew rate;

- the noise performance. This is normally determined by a combination of the source resistance (of the external source that is driving the amplifier) and the collector current. The lower the source resistance, the higher the I_c required for minimal noise;

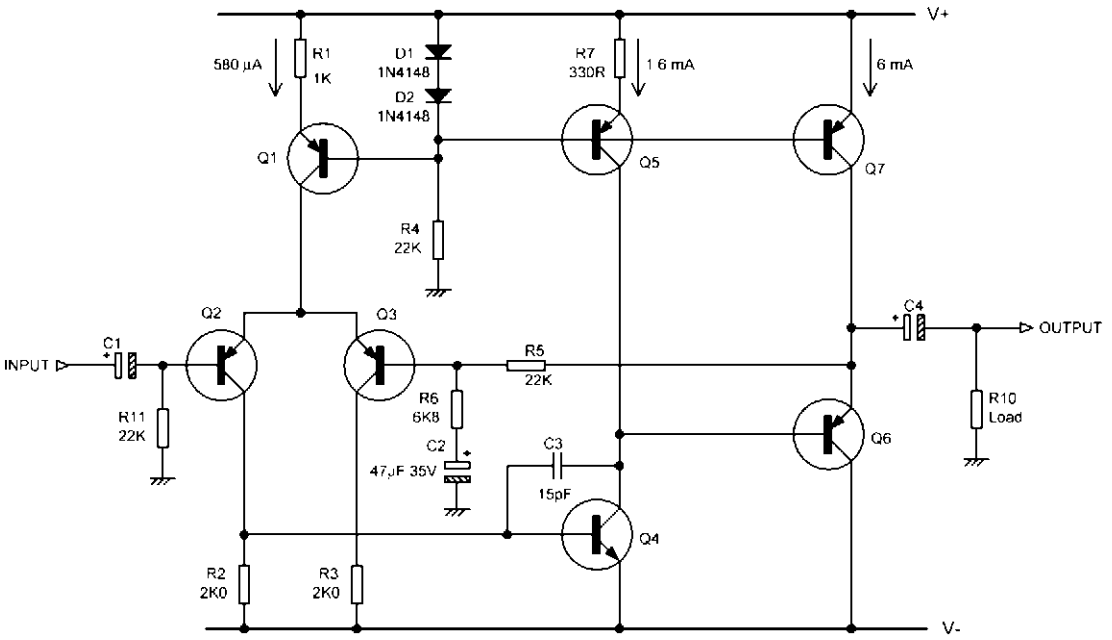

Figure 3.33: An improved discrete op-amp, with the input stage balanced and the output stage inverted to share the biasing diodes, and so reduce component count

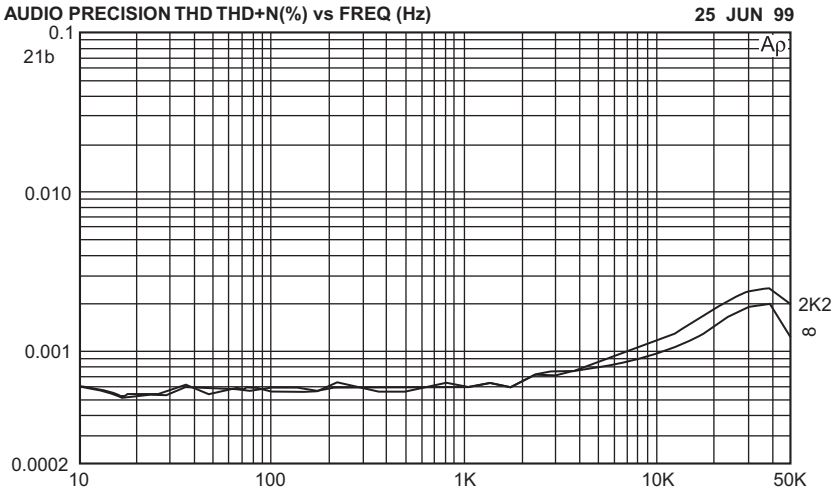

Figure 3.34: THD of the improved op-amp circuit, showing that the effect of a 2k2 load on linearity is small. Output level 8 Vrms

- the input bias currents, and hence DC accuracy in some circumstances. Input transistor beta also has a major influence on this.

A good example of discrete op-amp usage is a preamplifier I designed a while back [13].

High-Input-Impedance Bipolar Stages

Transistors are commonly thought of as low-impedance devices, but in fact they can be used to create amplifiers with extremely high input impedances. FETs are of course the obvious choice for high-input-impedance amplifiers, but their lack of transconductance is a drawback. This section was inspired by an article by T.D. Towers in 1968 that is still well worth reading [14]. The circuits that follow deliberately use high-voltage, low-beta transistors, as higher than normal rails are one of the reasons for using discrete circuitry – ±24V rails used. The impedances given were measured and also checked with SPICE.

Figure 3.35(a) shows a simple emitter-follower biased by R_{bias}, which at 100 kΩ is about as high as you would want it to be, because of the voltage drop due to the base current. That limits the input impedance to 100 kΩ of course. The First Principle of high-impedance design is to bootstrap the bias resistor as in Figure 3.35(a), which raises the input impedance to 500 kΩ. You may be wondering: why not more? One reason is that Q1 is only a simple emitter-follower and its voltage gain is distinctly less than 1, limiting the efficacy of the bootstrapping.

The Second Principle of high-impedance design with simple discrete stages is that any loading on the output reduces the input impedance because, as noted earlier:

$$R_{in} = \beta(R_e \| R_{load}) \qquad \text{(Equation 3.3)}$$

and the bootstrap capacitor C2 is driving the load of R1 even if there is no external loading. Adding an external 10 kΩ R_{load} to represent the following stage reduces the input impedance to 350 kΩ.

Having noted that both R_e and R_{load} pull down the input impedance, we will take steps to increase their effective values. Figure 3.35(b) shows R_e made very high by replacing the emitter resistor with a current source Q2. R_{load} is made high by adding simple emitter-follower Q3 to drive the bootstrap and the output. This gives a 6.1 MΩ input impedance even when driving an external 10 kΩ load output.

A further increase in input impedance can be obtained by increasing the β term in Equation 3.3, by using a Darlington configuration, where one emitter-follower feeds another, as in Figure 3.35(c). Q1 must have a reasonable collector current to operate at a good β – more than the base current of Q2. An emitter resistor to the negative rail would increase the loading and defeat the object, so R4 is used, with its lower end bootstrapped from the emitter of Q2. This

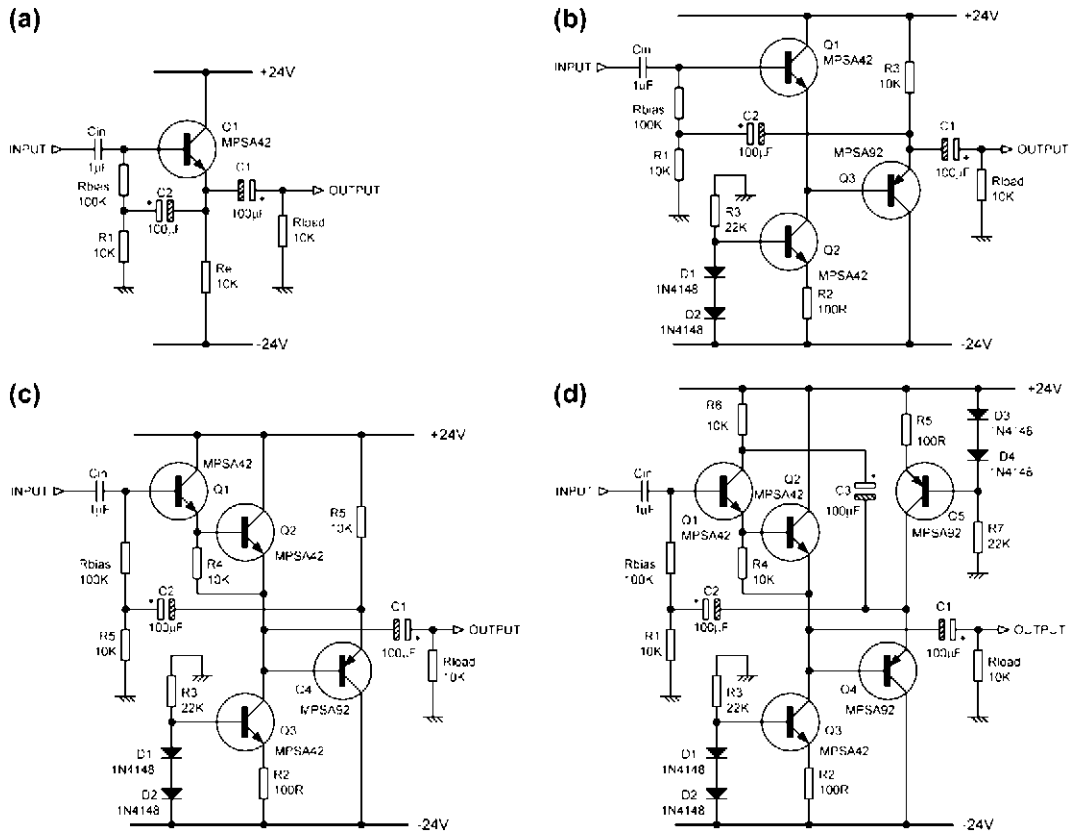

Figure 3.35: High-impedance input stages. (a) Simple emitter-follower with bootstrapped biasing. (b) Emitter-follower with current source and bootstrap driver stage. (c) Darlington with current source and bootstrap driver stage. (d) Darlington with current source and Q1 collector bootstrapped

technique is also used in power amplifier circuitry [15]. This gives an input impedance of 21 MΩ with an external 10 kΩ load. The output is now taken from the Q2 emitter once more.

To significantly further raise the input impedance, we need to take on board the Third Principle of high-impedance design: bootstrap the input transistor collector, as in Figure 3.35(d). The collector resistance r_c of Q1 and the base-collector capacitance c_{bc} are both effectively in parallel with the input; the former can also be regarded as Early effect causing I_b to vary. Their effects are reduced by bootstrapping Q1 collector using R6 and C3. (Note that collector bootstrapping cannot be used with a single-transistor stage [16].) The emitter-follower Q4 also has its emitter resistor replaced by current source Q5 to make its gain nearer 1 for more effective bootstrapping and help with driving R1 and R6. The output point has also been shifted back to the second emitter-follower. The result is an input impedance of 60 MΩ, or 50 MΩ with an external 10 kΩ load.

We have achieved this using only five transistors, so the BJT is clearly not an inherently low-impedance device. There are many more technical possibilities if you need a really astronomical input impedance; the record in 1968 appears to have been no less than 20,000 MΩ [17].

The circuits in Figure 3.35 are not optimized for linearity. They all give substantially more distortion when fed from a high source impedance such as 1 MΩ, as the base currents drawn are not linear.

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